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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,321	09/04/2003	Richard B. Watson JR.	200301955-2 (1662-37901)	5852

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
BARBEE, MANUEL L	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,321	WATSON ET AL.	
	Examiner	Art Unit	
	Manuel L. Barbee	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19,20,23,24,27,28,32-34,45,49,50,62-66 and 4549* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33,34 and 62* is/are allowed.

6)☒ Claim(s) *19,20,23,24,27,28,32,45,49,50,63,65 and 66* is/are rejected.

7)☒ Claim(s) *64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 19, 20, 23, 24, 45, 49, 50, 63 and 65 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelkar et al. (US Patent No. 5,663,991).

With regard to generating first and second reference clock signals, defining a time window and comparing a plurality of cycle of a target clock to the reference clock signals, as shown in claim 19, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition on an ASIC (col. 1, lines 13-27; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the time window and repeating the comparing and adjusting to determine the uncertainty window, as shown in claim 19, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35).

With regard to coupling the core clock to a first and a second adjustable delay chain to created two signals delayed by different amounts, as shown in claim 20, Kelkar et al. teach using different delay on each delay element (col. 3, line 67 - col. 4, line 54;

Fig. 2, 3). With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 23, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5). With regard to adjusting the time window, as shown in claim 24, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35).

With regard to generating four reference clock signals, defining three time bins and comparing a plurality of target clock signals with the reference clock signals, as shown in claim 45, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the time window and repeating the comparing and adjusting to determine the uncertainty window, as shown in claim 45, Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions, which would require repeating the comparing and adjusting (col. 6, lines 28-35).

With regard to defining the time window between corresponding rising edges of the first and second reference signal, as shown in claim 49, Kelkar et al. teach an alternate delay device that uses inverters, which would simply delay the reference clock by a small amount and therefore windows would be between rising edges (col. 5, line 46 - col. 6, line 35; Fig. 5). With regard to adjusting the time window, as shown in claim 50,

Kelkar et al. teach adjusting the delay of the delay elements to change the time slices and measuring the jitter under different conditions (col. 6, lines 28-35).

With regard to comparing a plurality of cycles of a target clock to a first and second reference clock to determine whether the target clock makes state transitions within a time window, as shown in claim 63, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). With regard to adjusting the phase of the first and second reference clock, wherein the phases are independently controlled, as shown in claim 63, Kelkar et al. teach adjusting the phase of the time slices and delay elements with controllable delay (col. 6, lines 28-35; col. 5, lines 46-61; Fig. 5m inverters 1-100).

With regard to a clock domain regions of an electronic device and a jitter measurement circuit with a plurality of independently controlled delay elements and a measurement unit for comparing the target clock to a plurality of reference clock signals, as shown in claim 65, Kelkar et al. teach generating five clock signals that create four time slices and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 27, 28, 32 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al. in view of Neudeck (US Patent No. 5,701,335).

With regard to a measurement circuit on the die of a microprocessor and a plurality of reference clocks with different phase and comparing a target clock to the time windows created by the reference clocks, as shown in claim 27, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which time slice the transition of the measured clock makes a transition on a built-in self measurement (Title; col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3). Kelkar et al. do no teach an external measurement system connected by way of a scan chain that executes software to control the measurement circuit and to adjust phase relationships of the reference clocks, as shown in claim 27. Neudeck teaches using a scan chain to control testing of integrated circuits (col. 1, lines 1-37; col. 2, lines 45-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include a scan chain for external control, as taught by Neudeck, because then components can be isolated for testing and debugging in larger systems (Neudeck; col. 1, lines 13-36).

With regard to a plurality of delay units and a measurement unit, as shown in claim 28, Kelkar et al. teach defining time slices with references signals each delayed by a different amount of time and measuring jitter of a clock by determining during which

time slice the transition of the measured clock makes a transition (col. 2, lines 15-35; col. 3, line 62 - col. 5, line 2; Fig. 3).

Kelkar et al. do not teach that the external measurement system has a microcontroller, as shown in claim 32. Neudeck teach test instructions and test data being communicated to a circuit being tested (col. 1, lines 13-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include a scan chain for external control, as taught by Neudeck, because then components can be isolated for testing and debugging in larger systems (Neudeck; col. 1, lines 13-36).

Kelkar et al. teach all the limitations of claim 65 upon which claim 66 depends. Kelkar et al. do not teach an external measurement system connected by way of a scan chain that executes software to control the measurement circuit and to adjust phase relationships of the reference clocks, as shown in claim 66. Neudeck teaches using a scan chain to control testing of integrated circuits (col. 1, lines 1-37; col. 2, lines 45-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the self measurement device, as taught by Kelkar et al., to include a scan chain for external control, as taught by Neudeck, because then components can be isolated for testing and debugging in larger systems (Neudeck; col. 1, lines 13-36).

Allowable Subject Matter

5. Claims 33, 34 and 62 allowed.

6. Claim 64 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: None of the prior art teach a method for calibrating a measurement circuit in a system for measuring on the die of the electronic device an uncertainty window that includes generating a first and second calibration signal each with the same frequency but differing in phase relationship by a known time, phase locking the output of a programmable delay chain to the first calibration signal and noting the number of taps required to phase lock the first calibration signal, phase locking the output of the programmable delay chain to the second calibration signal and noting the number of programmable taps required to phase lock the second calibration signal, attributing the difference in the number of taps to the known period of time and attributing each tap to a portion of the known period of time, as shown in claim 33. None of the prior art teaches a method comprising generating on a microprocessor die first and second reference clock signals having the same frequency but differing in phase relationship, defining a time window between features of the first and second reference clock signals, comparing a plurality of cycles of a target clock to the reference clock signals to determine whether the clock signal makes state transitions within the time window, adjusting the phase of only one of the first and second reference clock signals to adjust the time window and repeating the comparing and adjusting to determine an uncertainty window, as shown in claim 62.

Response to Arguments

8. Applicant's arguments filed 20 October 2004 have been fully considered but they are not persuasive. With regard to claims 19, 27 and 45, Applicant states that Kelkar fails to teach or suggest that the time window defined between the features of the first and second reference clock signal should be adjusted. Applicant states that Kelkar teaches a window that remains constant in the face of process variations, temperature differences and/or power supply voltage swings using a calibration circuit that works by forcing total delay to be equal to one period of the test clock. Although Kelkar teaches adjustment within a calibration system, the time delay of inverters and therefore the durations of time slices are changed during the calibration process (col. 6, lines 7-35). Adjustment of the time windows may be triggered by a change in the frequency of the test clock or by process variations.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Manuel L. Barbee whose telephone number is 571-272-2212. The examiner can normally be reached on Monday-Friday from 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mlb
November 15, 2004

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800